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10/616,647	07/09/2003	Hsilin Huang	VIA-P003	3445

7590 11/01/2007  
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Menlo Park, CA 94026-6402

EXAMINER
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GEIB, BENJAMIN P

ART UNIT	PAPER NUMBER
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2181

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11/01/2007

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

# Office Action Summary

Application No.

10/616,647

Applicant(s)

HUANG ET AL.

Examiner

Benjamin P. Geib

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 20 August 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-20 and 22-35 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-20 and 22-35 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 09 July 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 08/20/2007 has been entered.

### ***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-20 and 22-35 are rejected under 35 U.S.C. 102(e) as being anticipated by Arnold et al., U.S. Patent No. 6,438,681 (Herein referred to as Arnold).

4. Referring to claim 1, Arnold has taught a method of monitoring and controlling instruction dependency for microprocessors, the method comprising:

fetching an instruction at a thread control element [*register stage circuitry*; See FIG. 3] from an instruction buffer [*instruction dispersal unit*; FIG. 1, component 18] [The

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*register stage processing circuitry receives instructions from the instruction dispersal unit; column 3, lines 13-23, 44-47];*

comparing, with a comparator, one or more source operand identifications of the instruction at the thread control element outside of a pipeline stage or storage location to one or more temporary register identifications *[The register identifiers in the register stage are compared to the register identifiers of later stages (i.e. stages 28, 32, and 36); column 6, lines 50-66]*, wherein each thread control element and comparator forms a bi-directional correspondence, and wherein each of the one or more temporary register identifications is stored in a temporary register identification pipeline storage location of a set of one or more temporary register identification pipeline storage locations *[FIG. 3, components 89, 91, and 93; column 6, lines 50-66];*

verifying whether any of the one or more source operand identifications at the thread control element matches any of the one or more temporary register identifications *[column 6, line 66 – column 7, line 10];*

in response to a match of the source operand identification and the temporary register identification, prohibiting the instruction held in the corresponding thread control element from executing in that clock cycle, wherein the match corresponds to instruction dependency *[If there is a match then a data dependency exists (column 6, line 66 – column 7, line 10) and the instruction is stalled (column 4, lines 15-19)].*

5. Referring to claim 2, Arnold has taught the method of claim 1, wherein none of the one or more source operand identifications in the thread control element matches

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any of the one or more temporary register identifications *[column 6, line 66 – column 7, line 10]*.

6. Referring to claim 3, Arnold has taught the method of claim 2, further comprising the step of initiating execution of the instruction *[column 3, lines 44-49]*.

7. Referring to claim 4, Arnold has taught the method of claim 3, further comprising the step of verifying whether a destination operand of the instruction is a temporary register *[column 6, lines 35-66]*.

8. Referring to claim 5, Arnold has taught the method of claim 4, wherein the destination operand is not a temporary register *[column 6, lines 35-66]*.

9. Referring to claim 6, Arnold has taught the method of claim 5, further comprising the step of writing a null value into a first pipeline storage location of the set of one or more temporary register pipeline storage locations *[Since register identifiers follow their associated instructions down the pipeline (column 6, lines 35-49), if the instruction doesn't have a register identifier then a null value is inherently written into the first latch (FIG. 2, component 87)]*.

10. Referring to claim 7, Arnold has taught the method of claim 4, wherein the destination operand is a temporary register *[column 6, lines 35-66]*.

11. Referring to claim 8, Arnold has taught the method of claim 7, further comprising the step of writing an identification corresponding to the destination operand into a first pipeline storage location of the set of one or more temporary register pipelines *[The register identifier (i.e. identification corresponding to the destination operand) of the*

*instruction is written into the first latch (component 89) of the set of latches; See FIG. 3; column 6, lines 35-49].*

12. Referring to claim 9, Arnold has taught the method of claim 1, wherein the content in all except the last of the set of one or more temporary register pipeline storage locations is shifted to the next pipeline storage location at the beginning of each clock cycle *[column 6, lines 35-49].*

13. Referring to claim 10, Arnold has taught the method of claim 9, wherein the content of the last pipeline storage location of the set of one or more temporary register pipeline storage locations is released at the beginning of each clock cycle *[column 6, lines 35-49].*

14. Referring to claim 11, Arnold has taught the method of claim 1, wherein at least one of the one or more source operand identifications at the thread control element matches one of the one or more temporary register identifications *[column 6, line 66 – column 7, line 10].*

15. Referring to claim 12, Arnold has taught the method of claim 11, further comprising the step of prohibiting execution of the instruction *[If there is a match then a data dependency exists (column 6, line 66 – column 7, line 10) and the instruction is stalled (column 4, lines 15-19)].*

16. Referring to claim 13, Arnold has taught the method of claim 12, further comprising the step of comparing the one or more source operand identifications at the thread control element to the one or more temporary register identifications at the beginning of each clock cycle until none of the one or more source operand

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identifications matches any of the one or more temporary register identifications *[column 6, lines 50-66]*.

17. Referring to claim 14, Arnold has taught the method of claim 13, further comprising the step of verifying whether a destination operand of the instruction is a temporary register *[column 6, lines 35-66]*.

18. Referring to claim 15, Arnold has taught the method of claim 14, wherein the destination operand is not a temporary register *[column 6, lines 35-66]*.

19. Referring to claim 16, Arnold has taught the method of claim 15, further comprising the step of writing a null value into a first pipeline storage location of the set of one or more temporary register pipeline storage locations *[Since register identifiers follow their associated instructions down the pipeline (column 6, lines 35-49), if the instruction doesn't have a register identifier then a null value is inherently written into the first latch (FIG. 2, component 87)]*.

20. Referring to claim 17, Arnold has taught the method of claim 14, wherein the destination operand is a temporary register *[column 6, lines 35-66]*.

21. Referring to claim 18, Arnold has taught the method of claim 17, further comprising the step of writing an identification corresponding to the destination operand into a first pipeline storage location of the set of one or more temporary register pipeline storage locations *[The register identifier (i.e. identification corresponding to the destination operand) of the instruction is written into the first latch (component 89) of the set of latches; See FIG. 3; column 6, lines 35-49]*.

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22. Referring to claim 19, Arnold has taught a method of monitoring and controlling instruction dependency for microprocessor systems, the method comprising:

a) fetching an instruction at a thread control element *[register stage circuitry; See FIG. 3] [The register stage processing circuitry receives instructions from the instruction dispersal unit; column 3, lines 13-23, 44-47];*

b) receiving an instruction request at an arbiter, wherein the instruction request is issued from the thread control element *[Receiving an instruction at the instruction dispersal unit (FIG. 1, component 18); column 3, lines 13-23];*

c) comparing one or more source operand identifications of the instruction at the thread control element to one or more temporary register identifications *[The register identifiers in the register stage are compared to the register identifiers of later stages (i.e. stages 28, 32, and 36); column 6, lines 50-66],* wherein each of the one or more temporary register identifications is stored in a temporary register identification pipeline storage location of a set of one or more temporary register identification pipeline storage locations *[FIG. 3, components 89, 91, and 93],* and wherein said one or more source operand instructions at said thread control element is not part of a pipeline or pipelines *[the register stage circuitry is outside of the temporary register identification pipeline storage locations (comprising latches 89, 91, and 93; See FIG. 3)];*

d) verifying whether any of the one or more source operand identifications matches any of the one or more temporary register identifications *[column 6, line 66 – column 7, line 10];*

e) in response to a match of the source operand identification and the temporary register identification, prohibiting the instruction held in the corresponding thread control element from executing in that clock cycle, wherein the match corresponds to instruction dependency *[If there is a match then a data dependency exists (column 6, line 66 – column 7, line 10) and the instruction is stalled (column 4, lines 15-19)]*;

f) if none of the one or more source operand identifications matches any of the one or more temporary register identifications:

f1) verifying whether a destination operand of the instruction is a temporary register *[column 6, lines 35-66]*; and

f2) if the destination operand of the instruction is a temporary register: writing an identification corresponding to the destination operand into a first pipeline storage location of the set of one or more temporary register pipeline storage locations *[The register identifier (i.e. identification corresponding to the destination operand) of the instruction is written into the first latch (component 89) of the set of latches; See FIG. 3; column 6, lines 35-49]*;

f3) if the destination operand of the instruction is not a temporary register: writing a null value into a first pipeline storage location of the set of one or more temporary register pipeline storage locations *[Since register identifiers follow their associated instructions down the pipeline (column 6, lines 35-49), if the instruction doesn't have a register identifier then a null value is inherently written into the first latch (FIG. 2, component 87)]*.

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23. Referring to claim 20, Arnold has taught the method of claim 19, further comprising the step of initiating execution of the instruction *[column 3, lines 44-49]*.

24. Referring to claim 22, Arnold has taught the method of claim 19, if at least one of the one or more source operand identifications at the thread control element matches one of the one or more temporary register identifications in step e) *[column 6, line 66 – column 7, line 10]*, further comprising the steps of:

prohibiting the execution of the instruction *[If there is a match then a data dependency exists (column 6, line 66 – column 7, line 10) and the instruction is stalled (column 4, lines 15-19)]*;

reiterating step d) until none of the one or more source operand identifications matches any of the one or more temporary register identifications *[column 6, lines 50-66]*; and

verifying whether a destination operand of the instruction is a temporary register *[column 6, lines 35-66]*.

25. Referring to claim 23, Arnold has taught the method of claim 22, wherein the destination operand is a temporary register *[column 6, lines 35-66]*.

26. Referring to claim 24, Arnold has taught the method of claim 23, further comprising the step of writing an identification corresponding to the destination operand into a first pipeline storage location of the set of one or more temporary register pipeline storage locations *[The register identifier (i.e. identification corresponding to the destination operand) of the instruction is written into the first latch (component 89) of the set of latches; See FIG. 3; column 6, lines 35-49]*.

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27. Referring to claim 25, Arnold has taught the method of claim 22, wherein the destination operand is not a temporary register *[column 6, lines 35-66]*.

28. Referring to claim 26, Arnold has taught the method of claim 25, further comprising the step of writing a null value into a first pipeline storage location of the set of one or more temporary register pipeline storage locations *[Since register identifiers follow their associated instructions down the pipeline (column 6, lines 35-49), if the instruction doesn't have a register identifier then a null value is inherently written into the first latch (FIG. 2, component 87)]*.

29. Referring to claim 27, Arnold has taught the method of claim 19, wherein the content in all except the last of the set of one or more temporary register pipeline storage locations is shifted to the next pipeline storage location at the beginning of each clock cycle *[column 6, lines 35-49]*.

30. Referring to claim 28, Arnold has taught the method of claim 27, wherein the content of the last pipeline storage location of the set of one or more temporary register pipeline storage locations is released at the beginning of each clock cycle *[column 6, lines 35-49]*.

31. Referring to claim 29, Arnold has taught a system for instruction dependency monitor and control, comprising:

a set of one or more thread control elements for fetching instructions *[register stage circuitry; See FIG. 3] [The register stage processing circuitry receives instructions from the instruction dispersal unit; column 3, lines 13-23, 44-47]*, wherein said thread control elements are not part of a pipeline stage or pipeline storage location *[the register*

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*stage circuitry is outside of the temporary register identification pipeline storage locations (comprising latches 89, 91, and 93; See FIG. 3);*

a set of one or more comparing elements [*comparison logic; FIG. 3, component 24*], wherein each of the one or more comparing elements is directly coupled to a corresponding thread control element in the set of one or more thread control elements [*column 6, lines 50-66*]; and

a set of one or more temporary register identification pipeline storage locations [*latches; FIG. 3, components 89, 91, and 93*], wherein the one or more temporary register identification pipeline storage locations are directly coupled to the one or more comparing elements [*column 6, lines 50-66*].

32. Referring to claim 30, Arnold has taught the system of claim 29, further comprising an instruction buffer [*latch (FIG. 3, component 58)*] coupled to the one or more thread control elements [*column 6, lines 35-49*].

33. Referring to claim 31, Arnold has taught the system of claim 30, further comprising an arbiter [*instruction dispersal unit; FIG. 1, component 18*], wherein the arbiter is coupled to the one or more thread control elements, the one or more comparing elements, and the one or more temporary register identification pipeline storage locations [*See FIGs. 1 & 3; column 3, lines 13-23*].

34. Referring to claim 32, Arnold has taught the system of claim 31, further comprising an arithmetic logic unit (ALU) [*pipeline; FIGs. 1 & 3, component 21*] coupled to the arbiter [*column 3, lines 13-32*].

35. Referring to claim 33, Arnold has taught the system of claim 32, further comprising a set of one or more input data buffers *[latch (FIG. 3, component 58)]* coupled to the arbiter, wherein each input data buffer corresponds to a thread control element of the one or more thread control elements *[column 6, lines 35-49]*.

36. Referring to claim 34, Arnold has taught the system of claim 33, further comprising a set of one or more temporary register buffers *[the registers that are identified by the register identifiers]* coupled to the arbiter, wherein each temporary register buffer corresponds to a thread control element of the one or more thread control elements *[column 6, lines 35-49]*.

37. Referring to claim 35, Arnold has taught a system for instruction dependency monitor and control, comprising:

a set of one or more thread control elements for fetching instructions *[register stage circuitry; See FIG. 3] [The register stage processing circuitry receives instructions from the instruction dispersal unit; column 3, lines 13-23, 44-47]* wherein said thread control elements are not part of a pipeline stage or storage location *[the register stage circuitry is outside of the temporary register identification pipeline storage locations (comprising latches 89, 91, and 93; See FIG. 3)]*;

a set of one or more comparing elements *[comparison logic; FIG. 3, component 24]*, wherein each of the one or more comparing elements is directly coupled to a corresponding thread control element in the set of one or more thread control elements and wherein each thread control element and comparing element forms a bi-directional correspondence *[column 6, lines 50-66]*;

a set of one or more temporary register identification pipeline storage locations [latches; FIG. 3, components 89, 91, and 93], wherein the one or more temporary register pipeline storage locations are directly coupled to the one or more comparing elements [See FIG. 3; column 6, lines 50-66], and

an arbiter [instruction dispersal unit; FIG. 1, component 18] coupled to the thread control elements, the comparing elements, and the temporary register pipeline storage locations in each stage of a pipeline or pipelines [See FIGs. 1 & 3; column 3, lines 13-23].

### ***Response to Arguments***

38. Applicant's arguments filed 08/20/2007 have been fully considered but they are not persuasive.

39. Applicant argues the novelty/rejection of the claims, in substance that:

"Arnold does not teach of a comparator having any correspondence with a thread control element, let alone a bi-directional correspondence" (page 12)

"Neither does the cited reference teach of a thread control element outside of a pipeline stage or storage location" (page 12)

"Examiner has mistaken the thread control element for an instruction dispersal unit" (page 14)

"The reference cited does not state that a null value is written into a first pipeline storage location if the destination operand is not a temporary register" (page 15)

These arguments are not found persuasive for the following reasons:

The applicant argues that Arnold does not teach of a comparator having a bi-directional correspondence with a thread control element. As would be understood by one of ordinary skill in the art, a bi-directional correspondence indicates that both elements involved in the correspondence are in communication with each other (The

examiner notes that no definition is given in the applicant's specification for "bi-directional correspondence"). Arnold has taught thread control elements (i.e., register stage circuitry; the examiner notes that this is a different interpretation of Arnold from the previous Office Action) that communicate the register identifier of an instruction in the register stage to the comparison logic [Arnold; column 6, lines 50-62]. Arnold has further taught that the comparison logic determines if register dependencies exist [Arnold; column 6, line 66 – column 7, line 10] and, if so, prevents an instruction from moving out of the register stage [Arnold; column 4, lines 3-14]. Since the register stage circuitry is controlled based upon a determination made by the comparison logic, the comparison logic communicates with the register stage circuitry. Therefore, the register stage circuitry and the comparison logic have a bi-directional correspondence.

Regarding the applicant's argument that Arnold has not taught a thread control element outside of a pipeline stage or storage location, the examiner notes that the register stage circuitry is outside of the temporary register identification pipeline storage locations (comprising latches 89, 91, and 93; See FIG. 3). Therefore, Arnold has taught a thread control element outside of a pipeline stage or storage location.

The applicant argues that the examiner "has mistaken the thread control element for an instruction dispersal unit". Although the examiner disagrees with this characterization, this argument is moot in view of the examiner's new interpretation of Arnold (i.e. the thread control element is taught by the register stage circuitry).

Regarding the applicant's argument that Arnold has not taught that a null value is written into a first pipeline storage location if the destination is not a temporary register,

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the examiner notes that, since an instruction with a destination that is not a temporary register will not have a register identifier to write into the first pipeline storage location, the value written into the first pipeline storage location inherently be meaningless and unknown (i.e. null).

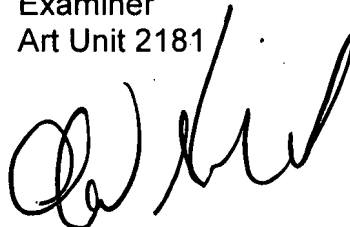
**Conclusion**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Benjamin P. Geib whose telephone number is (571) 272-8628. The examiner can normally be reached on Mon-Fri 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Benjamin P Geib  
Examiner  
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A handwritten signature in black ink, appearing to read 'Alford Kindred', is written over the printed name.

ALFORD KINDRED  
SUPERVISORY PATENT EXAMINER